ABSTRACT OF THE DISCLOSURE

Vertical MISFETs are formed over drive MISFETs and transfer MISFETs. The vertical MISFETs respectively comprise rectangular pillar laminated bodies each formed by laminating a lower semiconductor layer (drain), an intermediate semiconductor layer, and an upper semiconductor layer (source), and gate electrodes formed on their corresponding side walls of the laminated bodies with gate insulating films interposed therebetween. In each vertical MISFET, the lower semiconductor layer constitutes a drain, the intermediate semiconductor layer constitutes a substrate (channel region), and the upper semiconductor layer constitutes a source, respectively. The lower semiconductor layer, the intermediate semiconductor layer and the upper semiconductor layer are respectively comprised of a silicon film. The lower semiconductor layer and the upper semiconductor layer are doped with a p type and constituted of a p type silicon film.